Docket Number: 1902US

REMARKS

Claims 1-12, 14-20 are objected by the Examiner as being unpatentable over US 6,138,259 to Tsuto in view of US 4,965,799 to Green.

The Applicant amended these claims by introducing the feature "transferring data as data words having bit width which is multiple of the bit width of the input data". The above feature distinguish the present invention from the prior art systems on the reasons stated below.

As system speeds increased, all of these systems moved to multiple pattern generators. Figure 4 of Tsuto in US 6,138,259 describes such a system with two pattern generators (Claim 1, fourth part), and also accepts this is prior art (Fig 7 and 8 of the same patent). It is important to note that the result of this is a high speed data pattern. The high speed data pattern is input to the waveform shaping part (12) where it is converted to a high speed waveform.

The summary of the invention in Tsuto hinges on these multiple pattern generators: "In accordance with the present invention, the above object is attained by providing a semiconductor memory testing apparatus which comprises: ... a plurality of pattern generation parts ... and a high speed conversion part for multiplexing pattern data outputted from each of said plurality of pattern generation parts to obtain a high speed pattern signal."

The prior art requires the synchronisation of multiple pattern generators. This causes a problem in that the jitter of these multiple generators tends to be summed.

The present invention takes a different approach, using **a single very wide pattern generator (APG), with odd and even bits expressed using odd and even bits within the APG. These odd and even bits multiplexed together.** Thus, the synchronizing circuit functions differently.

Further, in the Examiner's opinion, Fig. 4 of Tsuto shows a data transmitting apparatus (12), which, according to the present invention comprises a plurality of data

transferring sections, while the unit designed by reference sign 12 in Fig. 4 is a waveform shape and does not comprise a plurality of data transferring sections (21A, 21B).

Further, according to the Examiner, Green in US 4,965,799 teaches variable frequency test clock.

However, the term "variable" is not the same as "programmable", as far as it regards the programmability of the test frequency. The main feature of the invention is to program the frequency so that it corresponds to the rate of data from the APG which can be varied, while the ratio of multiplexing remains the same. Furthermore, it is not only full frequency and low frequency that shall be programmed. Based on the specification, for example, **"for tester configuration purposes it is required that the system clock can be made synchronous to local bus clock in halted mode".** Further, **"when the bit is deasserted (SYS_CLOCK is disabled), the half-frequency clock (F/2) is switched to Local Bus clock, thus allowing configuring the tester; the full-frequency clock (F) is disabled."**

Thus, the term "programmable frequency" according to the invention is not the same as "variable frequency" described by Green.

Taking into account the above, we propose the attached adjustment to the claims to make the distinction between the present invention and the Tsuto's teachings clear, and to narrow the scope of the invention.

The amendments to claims are based on the description, where possible, and partly, on Figures. Thus, in paragraph [0043] it is said that "Waveforms are stored in the waveform RAM 53 (shall be 43) as 32-bit words, one word per clock period at the DUT.:" While in Fig. 8, for example, it is shown that the data words for accessing DUT have bit width 16. This can serve as support for inclusion in claims the following wording: "data transferring apparatus for transferring data as data words having bit width which is a multiple M of the bit width of the input data." Other support can be also found in the description.

CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to contact the Applicant's representative directly using the details below.

Respectfully submitted,

ABROSIMOV, Igor Anatolievich

KLOTCHKOV, Ilya Valerievich

Contact person: Maria Nilova
Tel. + 7 (812) 595 4051
+ 7 (812) 314 5347
fax: +7 (812) 314 4569
e-mail: maria.nilova@patentica.com

Enclosure: Claim Listing